a flexible layer of dielectric material having an array of metal plated vias extending therethrough in sloped relationship to opposing surfaces thereof with said array of metal plated vias on one surface corresponding to said array of conductive pads on said chip die and with each of said vias terminating in a metal pad on each of said opposing surfaces with each said metal pad on said one surface electrically connected to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said surfaces of said flexible layer and connected by solder thereto.

REMARKS

Claims 1 - 7 and 9 - 22 are pending in this application. Claims 14 - 22 have been withdrawn from consideration.

It is noted that the Examiner's Office Action Summary Sheet indicates that Claims 1 - 13 are pending. However, it should be pointed out that Claim 8 was canceled by Applicants' October 15, 2002 amendment.

Claim 5 has been amended to make it more readable.

The Rejections

The Examiner has rejected Claims 1 - 6, 10, 11, and 12 under 35 USC 103(a) as being unpatentable over Fox, et al. '878 and Alcoe (U.S. 2002/0046856) in combination with Okinaga (JP63-52432).

It is apparently the Examiner's position in the rejection of these claims that Fox, et al. meet all claim limitations except for the circuit card limitation, the sloped vias

limitation, the dielectric thickness limitation, the elastic modulus limitation and the copper plated vias limitation.

The Examiner has also rejected Claim 7 under 35 USC 103(a) as being unpatentable over Fox, et al. and Alcoe as applied to Claim 5, and further in combination with Sado (U.S. 4,330,165). The Examiner is relying on Sado for a teaching of the V-shaped metal plated vias limitation.

The Examiner has rejected Claim 9 under 35 USC 103(a) as being unpatentable over Fox, et al. and Alcoe as applied to Claim 6, and further in combination with Brodsky (U.S.5,984,691). Apparently, the Examiner is relying on Brodsky for a teaching of the array of holes between an array of copper plated vias limitation.

Finally, the Examiner has rejected Claim 13 as unpatentable over Fox, et al. and Alcoe as applied to Claim 6, and further in combination with Isaacs, et al. (U.S. 5,275,330). The Examiner is relying on Isaacs, et al. for a teaching of the plated vias filled with solder limitation.

The Examiner's Response to Applicants' Prior Arguments

The Examiner notes that Applicants have pointed out in their last amendment that Fox, et al. deal with another problem than Applicants. The Examiner states, however, that "the fact that Applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious" (emphasis added). The Examiner cites Ex parte Obiaya in support of this position.

Applicants would first like to point out that the Examiner's position is premised upon a conclusion that the differences between Fox, et al. and Applicants' invention are

obvious. The use of sloped vias is not taught or even suggested by Fox, et al. and, given what Fox, et al. are trying to achieve, would not otherwise be obvious. As will be explained more fully hereinafter, the sloped vias provide additional freedom of movement not provided or needed by Fox, et al. and, thus, the structural and functional differences between Applicants' invention and Fox, et al. are not simply something that "would flow naturally from following the suggestion of the prior art".

In fact, it is not clear to Applicants to what suggestion of Fox, et al. the Examiner is referring. Fox, et al. only suggest using a compliant interposer in an environment distinct from Applicants' environment. Fox, et al. do not suggest sloped vias to facilitate additional freedom to flex both horizontally and vertically and such would not naturally flow from Fox, et al. given the Fox, et al. packaging arrangement. The Examiner's reference to Ex parte Obiaya is noted but not considered relevant to the facts here. Applicants are not reciting an additional advantage associated with doing what the prior art suggests in an otherwise unpatentable invention. The claims recite structural distinctions (sloped-vias) over Fox, et al. which are patentable distinctions that act to facilitate horizontal and vertical movement which is a function not taught by Fox, et al. and such function would seem to be counter to the interests of Fox, et al. Obviously, without such structure as recited in Applicants' claims, no such so-called "additional advantage", would naturally flow from Fox, et al., and, in fact, it does not appear that such improved function would even be desirable in the Fox, et al. package, as will be pointed out hereinafter.

The Fox et al. Reference

As can be seen from the Fox, et al. background description, Fox, et al. are directed to overcoming the problems encountered in a chip on tape assembly (TAB) wherein a high concentration of supply current contact points around the chip perimeter and the associated clustered conductor runs on the lead frame (tape) act to create high inductance power connections between chip and substrate (see col. 1, line 48 et seq.). Fox, et al. also point out that the delivery of power to the peripheral contacts of a TAB-type chip assembly may also create additional problems, such as, electromigration failure (col. 1, line 62, et seq.). As further stated by Fox, et al., the high concentration of contact points also generates a significant amount of heat which heat is removed by Fox, et al. via a heat sink arrangement.

Fox, et al. overcome the above problems by rearranging the power delivery approach. Thus, "instead of providing power to closely-spaced peripheral contacts of a chip by way of a lead frame, some or all of these voltages are delivered to more widely spaced-apart power contacts on the face of the chip by way of a special compliant interposer which simultaneously urges the chip into intimate heat-exchange contact with a thermal transfer member or heat-sink engaging the backside of the chip" (col. 2, lines 1 et seq.).

Thus, the chip 16 of Fox, et al. is mounted in an opening 18a at the center of a flexible lead frame or tape 18, as shown in Figure 1. As stated in col. 2, line 59, et seq., "sandwiched between chip 16 and substrate 12 at site 24 thereon is a special compliant interposer 26 which simultaneously establishes certain electrical connections between chip 16 and substrate 12 and provides vertical compliance between the chip and substrate"

(emphasis added). Again, as stated in col. 3, line 58, et seq., the interposer 26 comprises "a compliant resilient pad or cushion 52 which conforms generally to the size and shape of chip 16, or at least to the area at the underside thereof encompassing the array of bumps 46".

To enhance the vertical compliance of interposer 26, Fox, et al. provide contacts that are cantilevered with the free ends arranged to engage solder bumps on the chip with such arrangement acting to reduce mechanical stresses on the chip (see col. 4, lines 33 et seq.). Again, in col. 4, line 61 et seq., Fox, et al. point out that the interposer "provides compliance for vertical tolerance which may exist due to warp or non-planarity between chip 16 and substrate 12" (emphasis added).

As shown in Figure 1, the Fox, et al. TAB assembly is held together mechanically by screws 34 that force heat sink 10 against chip 16 which heat sink, in turn, is forced against compliant member 26 which establishes power connections directly to the substrate therefor. The force provided by the screws is vertical and, thus, the resilience or flexing provided by compliant member 26 is, necessarily, vertical. Lateral or horizontal resilience is not needed and, in fact, it appears that given the clamped configuration, is neither possible nor desirable.

The Present Invention

As has been pointed out previously, Applicants' invention is directed to overcoming thermal expansion mismatch between chip and laminate chip carrier. It is known that flip chip applications require encapsulation to ensure a reliable flip chip interconnection in the solder joints and such encapsulation typically employs a high strength epoxy which acts to bond the chip to laminate chip carrier. It has been found that

this bonding of chip to laminate chip carrier reduces solder joint stress during thermal cycling but causes the chip itself to be put under cyclical high internal stress eventually leading to chip cracking, delamination and device breakdown.

The high internal stress has been attributed to the fact that the bonding of chip to laminate chip carrier acts to cause the composite material to act like a "bimetallic" element wherein the composite bends upon heating due to the different CTE value of the materials. As a result of the large thermal mismatch between chip and laminate chip carrier, the cyclical bending over time causes device failure.

To overcome the problem, Applicants employ a flexible and compliant interposer having an array of sloped metal plated vias. As stated on page 3 of Applicants' specification, "the floating interposer acts as chip carrier and provides stress relief to the electrical interconnections between chip die and circuit card by moving on its opposing surfaces relative to the CTE rate of the material with which it is in contact" (emphasis added). Thus, since thermal expansion movement is horizontal, i.e., in the plane of the materials, then compliance or flexing is provided by the interposer here in the horizontal direction.

Again, as stated on page 7 of Applicants' specification "the advantage of the sloped plated vias is that this configuration provides additional freedom to flex both vertically and horizontally. It is understood that the compliant interposer will readily flex or move in the vertical direction when no plated vias are present, but to facilitate flexing or movement in both the horizontal and vertical directions when vias are formed in the interposer, Applicants form the vias so as to slope with respect to the opposing surfaces of the interposer. It should be noted that, as stated on page 8, the sloped vias of Applicants'

Figure 4 not only act to provide "additional freedom to flex in both the vertical and horizontal directions but has the additional advantage of positioning pads 19 and 21 in vertical alignment with one another".

Distinctions Between Applicants' Invention and Fox, et al.

As stated above, the Fox, et al. arrangement acts to flex in the vertical direction and Fox, et al. facilitates this in one embodiment by providing cantilevered contacts. Since Fox, et al. has not addressed horizontal flexing it is obviously not of concern. Moreover, Fox, et al. cannot, and have no need to, flex in the horizontal direction. In this regard, Fox, et al. are not concerned about differences in thermal expansion of the materials employed and thermal mismatch.

Accordingly, since horizontal flexing is not a concern with Fox, et al. and, in fact, apparently not possible or even desirable, then Fox, et al. would have no reason to employ sloped vias which provide additional freedom to flex both vertically and horizontally. Moreover, even, arguendo, Fox, et al. would desire to flex both vertically and horizontally, the sloped via arrangement claimed by Applicants' acts to provide improved flexing neither taught nor suggested by Fox, et al. Given the cantilevered contacts 56 and wire bundles 76 of Fox, et al., it is not clear to applicants how Fox, et al. would employ sloped vias, or if sloped vias were somehow employed, how they would work to facilitate flexing, as taught by Applicants.

In this regard, the Examiner has stated in the rejection of Claims 1 - 6, 10, 11 and 12 that "it would have been obvious to one of ordinary skill in the art form sloped vias in the insulating material of Fox, et al. in order to reduce capacity and inductance as taught by Okinaga".

It should be pointed out, firstly, that Applicants are not employing sloped vias to reduce capacity and inductance. Again, Applicants are employing sloped vias to facilitate both horizontal and vertical flexing of the elastic dielectric material. Okinaga does not teach this and Fox, et al. does not teach this. In fact, it is not clear whether the Okinaga dielectric material is even elastic. Okinaga uses sloped vias for entirely different reasons than Applicants' use of sloped vias.

It is also not clear how the vias of Fox, et al. would be sloped given their cantilevered contact arrangement. In addition, if sloped vias were, indeed, somehow incorporated into Fox, et al., it is not clear how they would respond to the compression force employed by Fox, et al. in securing their heat sink, chip and interposer and substrate together via screws 34. It would appear that the combination of cantilevered contacts, slope vias and compressional force would render the Fox, et al. arrangement inoperative, or at least not operative in the manner intended by Fox, et al.

Accordingly, Applicants do not believe there would be any reason or motivation for one skilled in the art to use the sloped vias of Okinaga in Fox, et al. given the different packaging arrangements employed in these two references. It is clearly not a simple matter of using the sloped vias of Okinaga in Fox, et al., and even if somehow sloped vias were employed in Fox, et al., the vias would facilitate both horizontal and vertical flexing since Fox, et al., do not flex in both the horizontal and vertical directions.

The Examiner states that with respect to Claims 4 and 12, "absent evidence of criticality, it would have been an obvious matter of design choice to form the thickness of the dielectric to be 10 to 15 mils, since such a modification would have involved a mere change in size of a component". Applicants would like to point out that the flexible

interposer claimed with sloped vias is not a simple component of some larger combination but rather the flexible interposer with sloped vias is a central feature of the invention. The cases cited by the Examiner go to different facts than are presented here and involve mere changes in size as the only distinguishing feature of the claimed invention under rejection.

The Examiner has rejected Claim 7 under 35 USC 103(a) as unpatentable over Fox, et al. and Alcoe as applied to Claim 5, and further in combination with Sado.

The Sado interconnector is designed to overcome the problem of stretching of the rubber matrix due to the pressure required to obtain reliable connection between the two circuit boards. To limit this stretching, Sado employs at least one sheet member having a higher rigidity than the rubber matrix attached thereto. To provide additional rigidity, Sado uses curved linear conductive bodies 2 which make connection between circuit boards. As stated by Sado in col. 3, line 52, et seq. "the configuration of the linear conductive bodies ... is not necessarily straightforward but may be curved or bent". Sado goes on to state that "such a curved or bent configuration is rather preferable since the elastic resilience of the linear bodies can be effectively utilized when the interconnector is mounted between the two circuit boards" (emphasis added).

Thus, it appears that Sado is bending the conductive bodies to add resilience to the rubber matrix which is consistent with Sado's overall objective of adding resilience to the rubber matrix so as to avoid the problems incident stretching. Sado, then, is using what might loosely be called a V-shaped conductor to increase the resilience of the elastic material while Applicants are using this shape to facilitate resilience, i.e., decrease resilience.

The Examiner states that it would be obvious "to form the through hole of Fox, et al. V-shaped in order to facilitate absorption". This is apparently not what Sado is doing, i.e., facilitating absorption. Again, Sado rather appears to be increasing absorption of his elastic material, consistent with his objectives of overcoming the stretching problem.

Given what Sado is doing with his "V-shaped" conductors and given the fact that Fox, et al. facilitate only vertical absorption and do so with cantilevered contacts, there would be no reason to combined the teachings of Sado in Fox, et al. Moreover, as was the case with Okinaga, it is not at all clear how the teachings of Sado would be embodied in Fox, et al. given the Fox, et al. package structure. Again, if somehow the "V-shaped" arrangement of Sado were embodied in Fox, et al., it is not clear that Fox, et al. would be operative in the manner intended by Fox, et al.

The Examiner has, again, made reference in the outstanding rejection to the particular dimensions of a sloped via or "V" shaped via. As pointed out in Applicants' last amendment, Applicants are not claiming any dimensions in regard to the sloped vias. If the Examiner still believes that Applicants are claiming dimensions in regard to the sloped vias, Applicants respectfully request that the Examiner identify the particular claims which so specify these dimensions.

The Examiner has rejected Claim 9 as being unpatentable over Fox, et al. and Alcoe as applied to Claim 6, and in further combination with Brodsky. The Examiner states that it would have been obvious to one of ordinary skill in the art to incorporate an array of holes in the interposer of Fox, et al. and Alcoe in order to reduce stress as taught by Brodsky.

It is not clear to Applicants what would happen if the so-called hole arrangement of Brodsky were incorporated into Fox, et al. In this regard, it should be noted that the "hole" arrangement in Brodsky is not "an array of holes ... positioned between an array of copper plated vias". Rather, Brodsky uses specifically placed apertures around each contact to allow the contact to flex. The apertures are elongated and curved to circumscribe the contact. The Brodsky arrangement is not an array of holes between vias that allows the flexible layer to further flex but rather is an arrangement of elongated and curved apertures circumscribing the contact that allows the contact to flex.

Thus, Brodsky does not teach Applicants' claimed invention as set forth in Claim 9 and, moreover, it is not clear how Brodsky could be incorporated into Fox, et al. to meet Applicants' claimed invention. If Brodsky were somehow incorporated into Fox, et al., it is also not clear whether Fox, et al. would operate in the manner intended by Fox, et al. or if, indeed, it would operate at all.

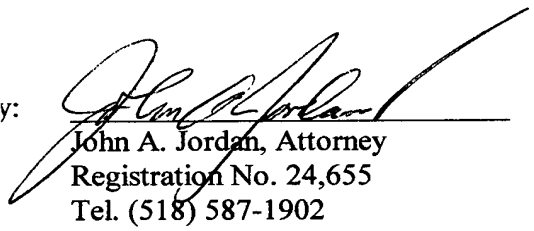
Attached hereto is a marked-up version of the changes made to Claim 5. The attached page is captioned **"VERSIONS WITH MARKINGS TO SHOW CHANGES MADE"**.

In view of Applicants' Remarks pointing out the claim distinctions over the prior art relied upon by the Examiner, Applicants firmly believe that the claims are now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejections, allow the claims as presented and pass

the case to issue.

Respectfully submitted,

Mark V. Pierson, et al.

By: 

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RAK/JAJ

"VERSION WITH MARKINGS TO SHOW CHANGES MADE".

5. (Twice Amended) An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough in sloped relationship to opposing surfaces thereof with said array of metal plated vias on one surface corresponding to said array of conductive pads on said chip die and with each of said vias terminating in a metal pad on each of said opposing surfaces with each said metal pad on said one surface [of said surfaces] electrically connected to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said surfaces of said flexible layer and connected by solder thereto.